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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,818	12/14/2004	Suk Hun Lee	3449-0413PUS1	8713

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/517,818	LEE, SUK HUN	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims **1-11** are rejected under 35 U.S.C. 102(e) as being anticipated by Emerson (US 6,958,497).

3. Regarding claim **1**, Emerson discloses in Fig 2 a nitride semiconductor LED, comprising: a substrate (10); a GaN-based buffer layer (11) formed on the substrate; $Al_yGa_{1-y}N$/GaN short period superlattice layers (16) formed on the GaN based buffer layer in a sandwich structure of upper and lower layers having an undoped GaN interposed therebetween; an first electrode layer of an n-GaN layer (lowest item 118) formed on the upper SPS layer; an active layer (125) formed on the first electrode layer; and a second electrode layer (32) of a p-GaN layer formed on the active layer.

4. Regarding claim **2**, Emerson discloses in Fig 1 the LED of claim 1, wherein the GaN buffer layer (11) has a super-lattice-structured $In_xGa_{1-x}N$/GaN laminated ($0 \leq x \leq 1$) (col 6 ln 58).

5. Regarding claim **3**, Emerson discloses in Fig 1 the LED of claim 1, further comprising the undoped GaN layer (within SPS 16) on the GaN based buffer layer.

6. Regarding claim **4**, Emerson discloses in Fig 2 a nitride semiconductor LED, comprising: a substrate (10); a GaN-based buffer layer (11) formed on the substrate; an indium-doped GaN layer (within SPS 16) formed on the GaN based buffer layer; $Al_yGa_{1-y}N$/GaN short period superlattice layers (16) formed on the indium-doped GaN layer in a sandwich structure of upper and lower layers having an undoped GaN interposed therebetween; an first electrode layer of an n+-GaN layer (within 16, see col 4 ln 60) formed on the upper SPS layer; an n-GaN layer (17) formed on the first electrode layer and containing a low concentration of dopants; an active layer (125) formed on the n-GaN layer; and a second electrode layer (32) of a p-GaN layer formed on the active layer.

7. Regarding claim **5**, Emerson discloses in Fig 1 the LED of claim 4, wherein the GaN buffer layer (11) has a super-lattice-structured $In_xGa_{1-x}N$/GaN laminated ($0 \leq x \leq 1$) (col 6 ln 58).

8. Regarding claim **6**, Emerson discloses in Fig 1 a nitride semiconductor LED, comprising: a substrate (10); a buffer layer (11) formed on the substrate; a first electrode layer (12) of an n+ GaN layer formed on the GaN based buffer layer and containing a high concentration of dopants; an n-GaN layer (16) formed on the first electrode layer and containing a low concentration of dopants; an active layer (18) formed on the n-GaN layer; and a second electrode layer (32) of a p-GaN layer formed on the active layer.

9. Regarding claim **7**, Emerson discloses the LED of claim 6, wherein the dopant concentration of the n+ GaN layer (12) is more than 1E18/cm^3 (col 7 ln 15).

10. Regarding claim **8**, Emerson discloses the LED of claim 6, wherein the dopant concentration of the n-GaN layer (16) is less than 1E18/cm^3 (col 7 ln 42).

11. Regarding claim **9**, Emerson discloses the LED of claim 6, wherein the dopant concentration of the n-GaN layer (16) is 1E17/cm^3 (col 7 ln 42).

12. Regarding claim **10**, Emerson discloses in Fig 1 the LED of claim 6, wherein the GaN buffer layer (11) has a super-lattice-structured $In_xGa_{1-x}N$/GaN laminated ($0 \leq x \leq 1$) (col 6 ln 58).

13. Regarding claim **11**, Emerson discloses in Fig 1 the LED of claim 6, wherein the super-lattice-structured laminated layer (16) comprises $Al_yGa_{1-y}N$/GaN layers formed on the buffer layer in a sandwich structure of upper and lower parts having an undoped GaN layer interposed therebetween ($0 \leq y \leq 1$).

14. Regarding claim **12**, Emerson discloses in Fig 2 a fabrication method of a nitride semiconductor LED, comprising: a growing up a GaN-based buffer layer (11) on a substrate (10); forming $Al_yGa_{1-y}N$/GaN short period superlattice layers (16) on the GaN based buffer layer in a sandwich structure of upper and lower layers having an undoped GaN interposed therebetween; forming a first electrode layer of an n+-GaN layer (within 16, see col 4 ln 60) containing a high concentration of dopants on the upper SPS layer; forming an active layer (125) on the first electrode layer; forming a second electrode layer (32) of a p-GaN layer on the active layer.

15. Regarding claim **13**, Emerson discloses in Fig 2 the LED of claim 12, further comprising the step of forming an n-GaN layer (within 16, see col 4 ln 60) containing a low concentration of dopants, between the first electrode layer of the n+ GaN layer and the active layer.

16. Regarding claim **16,** Emerson discloses in Fig 1 the fabrication method of claim 12, wherein the GaN buffer layer (11) has a super-lattice-structured $In_xGa_{1-x}N$/GaN laminated ($0 \leq x \leq 1$) (col 6 ln 58).

17. Regarding claim **17**, Emerson discloses in Fig 1 the method of claim 12, further comprising the step of forming an undoped GaN layer (within SPS 16) on the GaN based buffer layer.

18. Regarding claim **18**, Emerson discloses the method of claim 12, wherein the dopant concentration of the n+ GaN layer (12) is more than $1E18/cm^3$ (col 7 ln 15).

19. Regarding claim **19**, Emerson discloses the method of claim 13, wherein the dopant concentration of the n-GaN layer (16) is $1E17/cm^3$ (col 7 ln 42).

20. Regarding claim **20**, Emerson discloses in Fig 2 the method of claim 13, wherein the n-GaN layer (16) is formed with a semi-insulating layer (17).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims **14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson in view of Yuasa (US 6,017,774).

23. Regarding claim **14,** Emerson discloses the method of claim 12, wherein the layers are grown to a 50-400Å thickness, but does not specify that the GaN buffer layer is formed using MOCVD equipment at 500-800°C temperature and in an atmosphere having H_2 and N_2 carrier gases supplied while having TMGa, TMIn, TMAl source gas introduced and simultaneously having NH_3 gas introduced.

Yuasa teaches the formation of nitride films using MOCVD equipment at a growth temperature of 800°C (col 13 ln 66) in an atmosphere of H_2 and N_2 carrier gases supplied while TMGa and NH_3 are introduced simultaneously (col 13 ln 33). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Yuasa on the method of Emerson since the teachings produce a nitride film with good growth efficiency relative to the material supply amount (col 10 ln 20-23).

24. Regarding claim **15**, Emerson in view of Yuasa teach the method of claim 12, wherein the GaN buffer layer is grown with a 100 torr growth pressure (col 13 ln 56). Although neither teaches the flow rate of TMGa as between 5-300μmol/min, the rate would have been obvious to an ordinary artisan because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Where patentability is said to be based upon particular chosen dimensions or variables recited in a claim, the Applicant must show that the

chosen dimensions or variables are critical. See *In re Woodruff,* 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Koide discloses in Fig 1 each of the elements of claim 6. Tezen teaches formation of different buffer layers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCI

HOWARD WEISS
PRIMARY EXAMINER

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Examiner
Art Unit 2814